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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,514	11/25/2003	Masahiro Sunohara	031287	5140
23850	7590	08/02/2004	EXAMINER	
ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP			WILLIAMS, ALEXANDER O	
1725 K STREET, NW			ART UNIT	PAPER NUMBER
SUITE 1000				
WASHINGTON, DC 20006			2826	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/720,514	SUNOHARA ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Alexander O Williams	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### **Status**

- 1) Responsive to communication(s) filed on 5/21/04.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### **Disposition of Claims**

- 4) Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) 8-15 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-7 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### **Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### **Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### **Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____.   |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>5/27/ and 1/23/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____.                                   |

Serial Number: 10/720514 Attorney's Docket #: 031287  
Filing Date: 11/3/03; claimed foreign priority to 12/3/2002  
Applicant: Masahiro et al.

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 7), filed 5/21/04, has been acknowledged.

This application contains claims 8 to 15 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim 4 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, it is unclear and confusing to what is meant and what shows "a side surface of the via hole formed in the electronic parts except a bottom portion is covered with an inorganic insulating film." Where is this shown in the drawings?

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 and 2 are rejected under 35 U.S.C. § 102(e) as being anticipated by Umetsu et al. (U.S. Patent Application Publication # 2002/0127839A1).

1. Umetasu et al. (figures 1 to 10) specifically figures 8c, 9c and 10 show an electronic parts packaging structure, comprising: a wiring substrate (**shown as 5 in figure 9c and 80 in figure 10**) including a predetermined wiring pattern; an electronic parts **10**, a connection terminal **90,140** on an element forming surface of which is flip-chip **1** connected to the-wiring pattern; an insulating film **22** for covering the electronic parts; a

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via hole **24** formed in a predetermined portion of the electronic parts and the insulating film on the connection terminal; and an overlying wiring pattern **16** formed on the insulating film and connected to the connection terminal via the via hole.

2. An electronic parts packaging structure, according to claim 1, Umetasu et al. show wherein a side surface, of the via hole formed in the electronic parts and the insulating film constitutes a continued identical surface.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a through electrode and a connection terminal deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 3 to 7, **insofar as claim 4 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Umetsu et al. (U.S. Patent Application Publication # 2002/0127839A1).

3. Umetasu et al. (figures 1 to 10) specifically figures 8c, 9c and 10 show an electronic parts packaging structure comprising: a wiring substrate (**shown as 5 in figure 9c and 80 in figure 10**) including a predetermined wiring pattern; an electronic parts **10**, a connection terminal **90,140** on an element forming surface of which is flip-chip **1** connected to the wiring pattern, and the electronic parts having a through electrode **140** which is connected to the connection terminal via a first via hole **24** formed in the electronic parts, on a back surface; an insulating film **22** for covering the electronic parts; a second via hole (**continued 24 through 22**) formed in a predetermined portion of the insulating film on the through electrode; and an overlying wiring pattern **16** formed on the insulating film and connected to the through electrode via the second via hole.
4. An electronic parts packaging structure, according to claim 1, Umetasu et al. show wherein a side surface of the via hole formed in the electronic parts except a bottom portion is covered with an inorganic insulating film.
5. An electronic parts packaging structure, according to claim 1, Umetasu et al. show wherein the electronic parts is a semiconductor chip whose thickness is about 150 micrometers or less. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).
6. An electronic parts packaging structure, according to claim 1, Umetasu et al. show wherein a same structural body as the electronic parts, the insulating film, and the overlying wiring pattern, which are formed on the wiring pattern of the wiring substrate, is repeated n times (n is an integer of 1 or more) on as the overlying wiring pattern in a multi-layered fashion, and a plurality of electronic parts are connected mutually via the via hole (see figure 10).
7. An electronic parts packaging structure, according to claim 1, Umetasu et al. show wherein a connection terminal of an overlying electronic parts, is flip-chip connected to the overlying wiring pattern.

Therefore, it would have been obvious to one of ordinary skill in the art to use the thorough electrode and the connection terminal as "merely a matter of obvious engineering choice" as set forth in the above case law.

The listed references are cited as of interest to this application, but not applied at this time.

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Field of Search	Date
U.S. Class and subclass: 257/774,778,777,686,685,723,700,701,758	7/26/04
Other Documentation: foreign patents and literature in 257/774,778,777,686,685,723,700,701,758	7/26/04
Electronic data base(s): U.S. Patents EAST	7/26/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW  
7/27/04



Primary Patent Examiner  
Alexander O. Williams